IMPORTANT QUESTONS

Discuss the Memory Hierarchy in computer system with regard to Speed, Size and Cost.
Explain in detail about strobe control method of asynchronous data transfer.
Explain about arithmetic pipelining.
What is I/O interface and explain it with block diagram.
Describe the hardware implementation for addition and subtraction in detail.
Draw and explain about micro program control unit.

Discuss about addressing modes?
Explain the Memory-Reference instructions with examples.
With an example, explain Booth Multiplication algorithm.
Explain various Data Manipulation instructions with examples
Perform the arithmetic operation (+42)+(-13) and (-42)-(-13) in binary using signed 2's complement representation for negative numbers.
Write the major characteristics of RISC processors.

IMPORTANT BITS

1.	Which of the architecture is power efficient?			
	a) RISC	b) ISA	c) IANA	d) CISC

2.	In DMA transfers, the required signals and addresses are given by the _____			
	a) Processor	b) Device drivers	**c) DMA controllers**	d)None
3.	After the completion of the DMA transfer, the processor is notified by _____			
	a) Acknowledge signal	**b) Interrupt signal**	c) WMFC signal	d) None
4.	The DMA controller has _____ registers.			
	a) 4	b) 2	**c) 3**	d) 1
5.	The standard SRAM chips are costly as _____			
	a) Electronic devices	**b) 6 transistor per chip**	c) specially designed PCB's	d)a & b
6.	The drawback of building a large memory with DRAM is _____			
	a)) The large cost factor	b) The inefficient memory organization	**c) The Slow speed of operation**	d) All of the mentioned
7.	The ROM chips are mainly used to store _____			
	a) System files	b) Root directories	**c) Boot files**	d) Driver files
8.	The flash memories find application in _____			
	a) Super computers	b) Mainframe systems	c) Distributed systems	**d) Portable devices**
9.	The fastest data access is provided using _____			
	a) Caches	b)) DRAM's	c) SRAM's	**d) Registers**
10.	The SRAM's are basically used as _____			
	a) Registers	**b) Caches**	c) TLB	d) Buffer

1	A **Arithmetic** pipeline divides an arithmetic operation into sub operations for execution in the pipeline segments.
2	**Arbitration** must be performed to resolve multiple contention for the shared resources
3	To protect data from being changed simultaneously by 2 or more processors is called **Mutual exclusion**
4	The bus controller that monitors the cache coherence problem is referred as **Snoopy Cache Controller**
5	**Vector** processing deals with computations involving large matrices.
6	The Dynamic RAM consists of **Capacitors**
7	The transfer of data between main memory and cache memory is **Block**
8	The technique of segmentation suffers which fragmentation is **External**
9	The time taken to access a particular sector is **Latency Time**
10	The circuit which provides the interface between computer and similar interactive terminal is **UART**

ANSWERS

1 a
2 c
3 b
4 c
5 b
6 c
7 c

8 d
9 d
10 b

FILL IN THE BALANCE

1 Arithmetic
2 Arbitration
3 Mutual exclusion
4 Snoopy Cache Controller
5 Vector
6 Capacitors
7 Block
8 External
9 Latency time
10 UART

1.	When the R/W bit of the status register of the DMA controller is set to 1			
	a) Read operation is performed	b) Write operation is performed	c) Read & Write operation is performed	d) None
2.	A 16 X 8 Organization of memory cells, can store upto _____			
	a) 256 bits	b) 1024 bits	c) 512 bits	**d) 128 bits**
3.	The DMA transfer is initiated by _____			
	a) Processor	b) The process being executed	**c) I/O devices**	d) OS
4.	Circuits that can hold their state as long as power is applied is _____			
	a) Dynamic memory	**b) Static memory**	c) Register	d) Cache
5.	The address generated by processor is called to as a _____ address.			
	a) Physical	b) Logical	c) Virtual	**d) both b&c**

6.	Data channel is also called _____			
	a) CPU	b) DMA	**c) IO Processor**	d) None
7.	Data transfer to and from peripheral may be done by _____ mode.			
	a) Programmed I/O	b) Interrupt initiated I/O	c) DMA	**d) Above ALL**
8.	In an Asynchronous serial transmission, start bit always _____			
	a) 0	b) 1	c) group of 1's	d) none
9.	Instruction pipeline have _____ difficulty.			
	a) Resource conflict	b) data dependency	c)branch Difficulties	**d) Above ALL**
10.	In _____ organization, there are no specific I/O instructions.			
	a) Isolated	**b) Memory mapped**	c) DMA	d) none

1	Computer systems include special hardware components between CPU and peripheral unit is called **Interface** units.
2	In **Non-vectored** interrupt, the branch address is assigned to a fixed location in memory. Show Answer
3	The computer combines the Interface logic with DMA into one unit is called **I/O Processor**
4	The CPU activates the **Bus Grant** signal output to inform the external DMA that the buses are in the high impedance state.
5	The amount of processing that can be accomplished during a given interval of time is called **Throughput**
6	Distributed memory system is also referred to as **Loosely Coupled System**
7	A Bus that connects major components in a multiprocessor system such as CPU's, IOP's, and memory is called **System Bus**

8	**Vector Processing** is deals with computations involving large vectors and matrices.
9	UART stands for **Universal Asynchronous Receiver-Transmitter**
10	A Multiprocessor system with common shared memory is classified as **Tightly coupled System**

ANSWERS

1 a
2 d
3 c
4 b
5 d
6 c
7 d
8 a
9 d
10 b

Fill in the balance

1. Interface
2. Non-vectored
3. I/O Processor
4 Bus Grant
5 Throughput
6 Loosely Coupled System
7 System Bus
8 Vector Processing
9 Universal Asynchronous Receiver-Transmitter
10 Tightly coupled System